B

WE CLAIM AS OUR INVENTION:

~~Patent Claims~~

1. Integrated circuit arrangement

- whereby at least one doped region (3) is provided in a semiconductor substrate (1);
- whereby a plane with conductive useful structures (71) and at least one conductive filler structure (72) is arranged at the surface of the semiconductor substrate (1);
- whereby the conductive filler structure (72) is conductively connected to the doped region (3).

2. Circuit arrangement according to claim 1, whereby the conductive useful structures (71) and the conductive filler structure (72) exhibit essentially the same height and are surrounded by a planarizing insulation layer (11, 12).

3. Circuit arrangement according to claim 1 or 2, whereby the conductive filler structure (72) is connected to the doped region via a via hole and a contact (132).

4. Circuit arrangement according to claim 3, whereby the via hole overlaps the conductive filler structure (72) and the doped region (3), so that the surface of the conductive filler structure (72) and of the doped region (3) are in communication with the contact (132).

5. Circuit arrangement according to one of the claims 1 through 4, whereby the conductive useful structures (71) are gate electrodes and whereby the conductive filler structure (72) contains the material of the gate electrode.

6. Circuit arrangement according to one of the claims 1 through 5, whereby the doped region (3) is a doped well or the semiconductor substrate.

7. Circuit arrangement according to one of the claims 1 through 6,

- whereby a metallization level (16) is arranged above the plane wherein the conductive filler structure (72) is arranged;
- whereby the conductive filler structure (72) is connected to the metallization level (16) via a further contact.

8. Method for manufacturing an integrated circuit arrangement,

- whereby a doped region (3) is formed in a semiconductor substrate (1);
- whereby a plane having conductive useful structures (71) and at least one conductive filler structure (72) is formed on the semiconductor substrate (1) by application and structuring of a conductive layer (7);
- whereby an insulation layer (11, 12) is produced that surrounds and covers the conductive useful structures (71) and the conductive filler structure (72);
- whereby a conductive connection is produced between the conductive filler structure (72) and the doped region (3).

9. Method according to claim 8,
- whereby a via hole is opened in the insulation layer (11,12), said via hole respectively partially overlapping the conductive filler structure (72) and the doped region (3), so that the surface of the doped region (3) and of the conductive filler structure (72) is partially uncovered;
- whereby a contact (132) is formed in the via hole, said contact being in communication with the surface of the conductive filler structure (72) and of the doped region (3).

10. Method according to claim 8 or 9,
- whereby a metallization level (16) is produced above the plane wherein the conductive filler structure (72) is arranged;
- whereby a further contact (15) is produced via which the conductive filler structure is connected to the metallization level (16).